

FUNCTIONAL SPECIFICATION

for the

ADVANCED AMIGA CHIP SET (AA)

Contributors: S. Shanson

R. Raible

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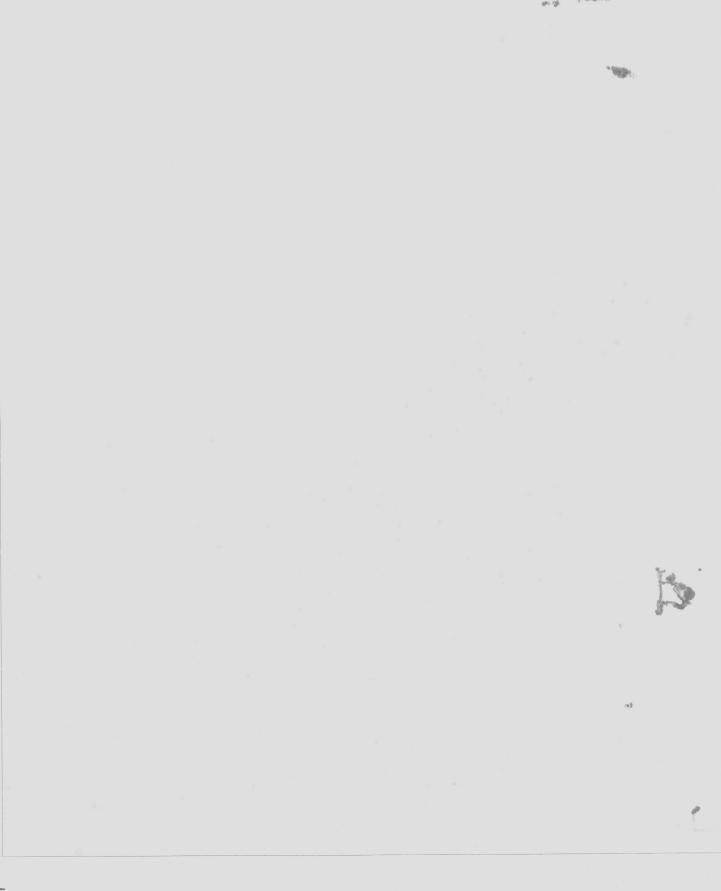
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PRELIMINARY

| 4/30/91 | added new LISAID definition |
|---------|--|
| 4/11/91 | added Spence's corrections. |
| 4/18/91 | added LISA sprite scan-doubling support. |
| 4/26/91 | added interlocks and Spence's mode list. |

New for AA

New for ECS



Summary of New features for AA

- 32 bit wide data bus supports input of 32-bit wide bitplane data and allows doubling of memory bandwidth. Additional doubling of bandwidth can be achieved by using Fast Page Mode Ram. The same bandwidth enhancements are available for sprites. Also the maximum number of bitplanes useable in all modes was increased to eight (8).
 - The Color Palette has been expanded to 256 colors deep and 25 bits wide (8 RED, 8 GREEN, 8 BLUE, 1 GENLOCK). This permits display of 256 simultaneous colors in all resolutions. A palette of 16,777,216 colors is available in all resolutions.
 - 28Mhz clock input allows for cleaner definition of HIRES and SHRES pixels. ALICE's clock generator is synchronized by means of LISA's 14MHz and SCLK outputs. Genlock XCLK and XCLKEN* pins have been eliminated (external MUX is now required).
 - A new register bit allows sprites to appear in the screen border regions (BRDRSPRT).
 - A bitplane mask field of 8 bits allows an address offset into the color palette. Two 4-bit mask fields do the same for odd and even sprites.
 - In Dual Playfield modes, 2 4-bitplane playfields are now possible in all resolutions.
 - Two Extra high-order playfield scroll bits allow seamless scrolling of up to 64 bit wide bitplanes in all resolutions. Resolution of bitplane scroll, display window, and horizontal sprite position has been improved to 35ns in all resolutions.
 - A new 8 bitplane HAM mode has been created, 6 for colors and 2 for control bits. All HAM modes are available in all resolutions (not just LORES as before).
 - A RST input pin has been added, which resets all the bits contained in registers that were new for ECS or LISA: BPLCON3, BPLCON4, CLXCON2, DIWHIGH, FMODE
 - Sprite resolution can be set to LORES, HIRES, SHRES, independent of bitplane resolution.
 - Attached Sprites are now available in all resolutions.
 - Hardware Scan Doubling support has been added for bitplanes and sprites. This is intended to allow 15KHz screens to be intelligently displayed on a 31KHz monitor, and share the display with 31KHz screens.

EXPLANATION OF NEW FEATURES

Bitplanes

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There are now 8 bitplanes instead of 6. In single playfield modes they can address 256 colors instead of just 64. As long as the memory architecture supports the bandwidth, all 8 bitplanes are available in all 3 resolutions. In the same vein, 4+4 bitplane dual playfield is available in all 3 resolutions, unless bitplane

scan-doubling is enabled, in which case both playfields share the same bitplane modulus register. Bits 15 thru 8 of BPLCON4 comprise an 8 bit mask for the 8 bit bitplane address, XOR'ing the individual bits. This allows the copper to exchange color maps with a single instruction. BPLCON1 now contains an 8 bit scroll value for each of the playfields. Granularity of scroll now extends down to 35nSec.(1 SHRES pixel), and scroll can delay playfield thru 32 bus cycles. Bits BPAGEM and BPL32 in new register FMODE control size of bitplane data in BPL1DAT thru BPL8DAT.

The old 6 bitplane HAM mode, unlike before, works in HIRES and SHRES resolutions. As before bitplanes 5 and 6 control its function as follows:

| BP6 | BP5 | RED | GREEN | BLUE |
|-----|-----|------------|------------------|--------|
| | | | | |
| 0 | 0 | select new | base register (1 | of 16) |
| 0 | 1 | hold | hold | modify |
| 1 | 0 | modify | hold | hold |
| 1 | 1 | hold | modify | hold |

There is a new 8 bitplane HAM (Hold And Modify) mode. This mode is invoked when BPU field in BPLCONO is set to 8, and HAMEN is set. Bitplanes 1 and 2 are used as control bits analagous to the function of bitplanes 5 and 6 in 6 bitplane HAM mode:

| BP2 | | BP1 | RED | | GREEN | | BLUE | |
|-----|---|-----|------------|------|--------|------|--------|--|
| | | | | | | | | |
| 0 | | 0 | select new | v ba | | er(1 | of 64) | |
| 0 | - | 1 | hold | | hold | | modify | |
| 1 | | 0 | modify | | hold | | hold | |
| 1 | | 1 | hold | | modify | | hold | |

Since only 6 bitplanes are available for modify data, the data is placed in the 6 MSB. The 2 LSB are left unmodified, which allows creation of all 16,777,216 colors simultaneously, assuming one had a large enough screen and picked one's base registers judiciously. This HAM mode also works in HIRES and SHRES modes.

For compatibility reasons EHB mode remains intact. Its existence is rather moot in that we have more than enough colors in the color table to replace its functionality. As before, EHB is invoked whenever SHRES=HAMEN=DPF=0, and BPU=6. Please note that starting with ECS DENISE there is a bit n BPLCON2 which disables this mode (KILLEHB).

Bits PF20F2,1,0 in BPLCON3 determine second playfield's offset into the color table. This is now necessary since playfields in DPF mode can have up to 4 bitplanes. Offset values are as defined in register map.

BSCAN2 bit in FMODE enables bitplane scan-doubling. When V0 bit of DIWSTRT matches V0 of vertical beam counter, BPL1MOD contains the modulus for the display line, else BPL2MOD is used. When scandoubled both odd and even bitplanes use the same modulus on a given line, whereas in normal mode odd bitplanes used BPL1MOD and even bitplanes used BPL2MOD. As a result Dual Playfield screens will probably not display correctly when scan-doubled.

Sprites

Bits SPAGEM and SPR32 in FMODE whether size of sprite load data in SPR0DATA(B) thru SPR7DATA(B) is 16,32, or 64 bits, analagous to bitplanes. BPLCON3 contains several bits relating to sprite behavior. SPRES1 and SPRES0 control sprite resolution, whether they

conform to the ECS standard, or override to LORES, HIRES, or SHRES. BRDRSPRT, when high, allows sprites to be visible in border areas. ESPRM7 thru ESPRM4 allow relocation of the even sprite color map. OSPRM7 thru OSPRM4 allow relocation of the odd sprite color map. In the case of attached sprites OSPRM bits are used.

SSCAN2 bit in FMODE enables sprite scan-doubling. When enabled, individual SH10 bits in SPRxPOS registers control whether or not a given sprite is to be scan-doubled. When V0 bit of SPRxPOS register matches V0 bit of vertical beam counter, the given sprite's DMA is allowed to proceed as before. If they don't match, then sprite DMA is disabled and LISA reuses the sprite data from the previous line. When sprites are scan-doubled, only the position and control registers need be modified by the programmer; the data registers need no modification.

NOTE: Sprite vertical start and stop positions must be of the same parity, i.e. both odd or both even.

Video

BYPASS bit in BPLCONO allows prioritized color address to bypass the color table and exit LISA on R(7:0) bus. SOGEN bit in BPLCON2 determines state of SOG output. This was intended to signal Video DAC chip (KELLY) to superimpose composite signal onto analog green output, but should come out on the video slot for custom video applications. Horizontal blanking registers HBSTART and HBSTOP have been added to LISA, eliminating the need for an external blanking input pin. There is now a BLANK output which allows the analog level for blanking to be different than black. This signal also should be included in a redefined video bus. BRDRBLNK bit in BPLCON3 allows the background to be BLACK and not the contents of COLOROO. Though the name of this bit is now a misnomer, I intend to leave the name intact.

Compatibility

RST_ pin resets all bits in all registers new to AA. These registers include: BPLCON3, BPLCON4, CLXCON2, DIWHIGH, FMODE.

ECSENA bit (formerly ENBPLCN3) is used to disable those register bits in BPLCON3 that are never accessed by old copper lists, and in addition are required by old-style copper lists to be in their default settings. Specifically, ECSENA forces the following bits to their default low settings:BRDRBLNK, BRDNTRAN, ZDCLKEN, EXTBLKEN, and BRDRSPRT. When ECSENA is set high again, the former settings for these bits are restored.

CLXCON2 is reset by a write to CLXCON, so that old game programs will be able to correctly detect collisions.

DIWHIGH is reset by writes to DIWSTRT or DIWSTOP. This interlock is inherited from ECS Denise.

Genlock Stuff

Lots of new genlock features were added to ECS DENISE and are carried over to LISA. ZDBPEN in BPLCON2 allows any bitplane, selected by ZDBPSEL2,1,0, to be used as a transparency mask (ZD pin mirrors contents of selected bitplane). ZDCTEN disables the old COLOR00 is transparent mode, and allows the bit31 position of each color in the color table to control transparency. ZDCLKEN generates a 14MHz clock synchronized with the video data that can be used by video post-processors. Finally, BRDNTRAN in BPLCON3 generates an opaque border region which can used to frame live video.

Color Lookup Table

The color table has grown from 32 13-bit registers to 256 25-bit registers. Several new register bits have been added to BPLCON3 to facilitate loading the table with only 32 register addresses. LOCT, selects either the 16 MSB or LSB for loading. Loading the MSB always loads the LSB as well for compatibility, so when 24 bit colors are desired load LSB after MSB. BANK2,1,0 select 1 of 8 32 address banks for loading as follows:

| BANK2 | 1 | BANK1 | 1 | BANK0 | 11 | Color | Add: | ress | Rang | e |
|---------|---|-------|---|-------|-----|---------|------|------|------|---|
| 0 | 1 | 0 | 1 | 0 | 11 | COLOR0 | 0 - | COL | OR1F | |
| 0 | i | 0 | i | 81 | H | COLOR2 | | | | |
| 0 | 1 | 1 | İ | 0 | 11 | COLOR4 | 0 - | COL | OR5F | |
| 0 | i | 1 | i | 1 | 11 | COLOR 6 | 0 - | COL | OR7F | |
| 1 | i | 0 | i | 0 | 11 | COLOR8 | 0 - | COL | OR9F | |
| 1 | 1 | 0 | 1 | 1 | 11 | COLORA | .0 - | COL | ORBF | |
| 1 | İ | 1 | i | 0 | 11 | COLORC | 0 - | COL | ORDF | |
| NE THAT | İ | 1 | 1 | 1 | 11: | COLORE | 0 - | COL | ORFF | |

RDRAM bit in BPLCON2 causes LISA to interpret all color table accesses as reads.

Note: There is no longer any need to "scramble" SHRES color table entries. This artifice is no longer required and people who bypass ECS graphics library calls to do their own 28MHz graphics are to be pointed at and publicly humiliated.

Collision

A new register CLXCON2 contains 4 new bits. ENBP7 and ENBP6 are the enable bits for bitplanes 7 and 8, respectively. Similarly, MVBP7 and MVBP8 are their match value bits. CLXDAT is unchanged.

Horizontal Comparators

All programmable comparators with the exception of VHPOSW have 35nSec resolution.:DIWHIGH, HBSTRT, HBSTOP, SPRCTL, BPLCON1. BPLCON1 has additional high-order bits as well. Note that horizontal bit position representing 140nSec resolution has been changed to 3rd least significant bit, where before it used to be a field's LSB. For example, bit 00 in BPLCON1 used to be named PF1HO and now it's called PF1H2.

Mouse/Joysticks

A two pin serial mouse interface replaces the 4 pin CCK multiplex scheme. This change is transparent to the programmer and allows 8 extra bits to be shifted in as well. These are displayed in the 8 MSB of LISAID and are intended for hardware configuration information. The mouse counters are updated only 1/16 as often as before (223 KHz), but this should be transparent to the user.

Coercion of 15KHz to 31KHz

We have added new hardware features to LISA to aid in properly displaying 15KHz and 31KHz viewports together on the same 31KHz display. LISA can globally set sprite resolution to LORES, HIRES, or SHRES. LISA will ignore SH10 compare bit in SPRxPOS when scan-doubling, thereby allowing ALICE to use these bits to individually set scan-

List of Registers ordered by Address

```
Symbols Used:
&=Register used by DMA channel only.
%=Register used by DMA channel usually, processors sometimes.
+=Address register pair.Low word uses DB1-DB15, High word DB0-DB4.
~=Address not writable by the Coprocessor unless COPCON bit 1 is set true.
h=new for HiRes chip set
p=new for IAA chip set
A=Agnus/Alice chip, D=Denise/Lisa chip, P=Paula chip
W=Write, R=Read,
ER=Early read. This is a DMA data transfer to RAM, from either the Disk
   or from the Blitter . Ram timing requires data to be on the bus
   earlier than microprocessor read cycles. These transfers are therefore
   initiated by Agnus timing, rather than a read address on the
   register address bus (RGA).
S=Strobe (write address with no register bits)
PTL, PTH=20 bit Pointer that addresses DMA data. Must be reloaded by a processor
    before use (Vertical blank for Bit Plane and Sprite pointers, and
prior to starting the Blitter for Blitter pointers). (old chips- 18 bits) LCL, LCH=20 bit Location (starting address) of DMA data. Used to automaticall restart pointers, such as the Coprocessor program counter (during
    vertical blank), and the Audio sample counter (whenever the audio length count is finished) (Old chips- 18 bits)
MOD=15 bit Modulo. A number that is automatically added to the memory address
    at the end of each line to generate the address for the beginning of
    the next line. This allows the Blitter (or the Display Window) to
    operate on (or display) a window of data that is smaller than the
    actual picture in memory. (memory map) Uses 15 bits, plus sign extend.
```

| NAME | tid La | ADDR | R/W | СНІ | P(s) | FUNCTION BOLLEGO |
|---|-------------|--|---------------------------------|-----------------------|-------------------|--|
| BLTDDAT DMACONR VPOSR VHPOSR DSKDATR JOYODAT JOY1DAT CLXDAT ADKCONR POTODAT POTINP SERDATR DSKBYTR | F.J. C. | ~000 ~002 ~004 ~006 ~008 ~00A ~00C ~00E ~010 ~012 ~014 ~016 ~018 ~01A | R R R R R R R | A A A | P D D P P P P P P | Blitter dest. early read (dummy address) DMA control (and blitter status) read Read Vert most sig. bits (and frame flop) Read Vert and horiz Position of beam Disk data early read (dummy address) Joystick-mouse 0 data (vert, horiz) Joystick-mouse 1 data (vert, horiz) Collision data reg. (Read and clear) Audio, disk control register read Pot counter pair 0 data (vert, horiz) Pot counter pair 1 data (vert, horiz) Pot pin data read Serial Port Data and Status read Disk Data byte and status read |
| INTENAR INTREQR DSKPTH DSKLEN DSKLEN DSKDAT REFPTR VPOSW VHPOSW COPCON SERDAT SERPER POTGO JOYTEST STREQU STRVBL STRHOR | + & & | ~01C ~01E ~020 ~022 ~024 ~026 ~028 ~02A ~02C ~032 ~034 ~036 ~038 ~03A ~03C | W W W W W S S | A A A A A | P P P P D D D P P | Interrupt Enable bits Read Interrupt Request bits read Disk pointer (High 5 bits) Disk pointer (Low 15 bits) Disk length Disk DMA Data write Refresh pointer Write Vert most sig. bits (and frame flop) Write Vert and horiz Position of beam Coprocessor control register (CDANG) Serial Port Data and stop bits write Serial Port Period and control Pot count start,pot pin drive enable and data Write to all 4 Joystick-mouse counters at once. Strobe for horiz sync with VB and EQU Strobe for horiz sync with VB (Vert. Blank) Strobe for horiz sync |

```
Strobe for identification of long horz. line.
         & ~03E S
                           D
STRLONG
                                  Blitter control register 0
BLTCON0
           ~040 W
BLTCON1
             ~042 W
                        A
                                  Blitter control register 1
             ~044 W
                                  Blitter first word mask for source A
BLTAFWM
                        A
BLTALWM
             ~046 W
                        A
                                  Blitter last word mask for source A
                                  Blitter Pointer to source C (High 5 bits)
           + \sim 048 W
BLTCPTH
                         A
                                  Blitter Pointer to source C (Low 15 bits)
           + ~04A W
BLTCPTL
                         A
                                  Blitter pointer to source B (High 5 bits)
           + ~04C W
BLTBPTH
                         A
                                  Blitter pointer to source B (Low 15 bits)
           + ~04E W
                         A
BLTBPTL
          + ~050
                   W
                                  Blitter Pointer to source A (High 5 bits)
                        A
BLTAPTH
                                  Blitter Pointer to source A (Low 15 bits)
          + ~052
                   W
                        A
BLTAPTL
                                  Blitter Pointer to destn. D (High 5 bits)
           + ~054
                   W
                         Α
BLTDPTH
                                  Blitter Pointer to destn. D (Low 15 bits)
           + ~056 W
                         A
BLTDPTL
                                 Blitter start and size (window width, height)
Blitter control 0 lower 8 bits (minterms)
Blitter V size (for 15 bit vert size)
Blitter H size & start (for 11 bit H size)
Blitter Modulo for source C
Blitter Modulo for source B
             ~058 W
                        A
BLTSIZE
           h ~05A W
                        A
BLTCON0L
                   W
           h ~05C
                        A
BLTSIZV
           h ~05C W
h ~05E W
~060 W
~062 W
~064 W
~066 W
BLTSIZH
                        A
BLTCMOD
                        A
                        A
BLTBMOD
                                  Blitter Modulo for source A
BLTAMOD
                        A
                        A
                                 Blitter Modulo for destn. D
BLTDMOD
             ~068
             ~06A
             ~06C
             ~06E
                                  Blitter source C data reg
           & ~070 W
BLTCDAT
                        A
                                  Blitter source B data reg
           & ~072 W
                       A
BLTBDAT
                                  Blitter source A data reg
           & ~074
BLTADAT
                   W
                         A
             ~076
                                  ext logic UHRES sprite pointer & data identifier
           &h 078 W
SPRHDAT
                         A
             ~07A ???????????????????????????????????
(BPLHDAT)
                                  Chip Revision level for Denise/Lisa
                   R
           h ~07C
                           D
LISAID
                                  Disk sync pattern register for disk read.
             ~07E
                    W
DSKSYNC
                                  Coprocessor first location reg (High 5 bits)
              080
                    W
COP1LCH
           +
                                  Coprocessor first location reg. (Low 15 bits)
               082
COP1LCL
           +
                    W
                         Α
               084 W
                                  Coprocessor second location reg. (High 5 bits)
                         A
COP 2 L CH
           +
                                  Coprocessor second location reg(Low 15 bits)
               086 W
                         A
COP 2 LCL
           +
                                  Coprocessor restart at first location
               088 S
                         A
COPJMP1
                                  Coprocessor restart at second location
               08A S
                         A
COP JMP 2
                                  Coprocessor inst. fetch identify
               08C W
                        A
COPINS
                                  Display Window Start (upper left vert-hor pos)
Display Window Stop (lower right vert-hor pos)
               08E W
                        A D
DIWSTRT
DIWSTOP
               090 W
                        A D
                                  Display bit plane data fetch start (hor pos)
Display bit plane data fetch stop (hor pos)
DMA control write (clear or set)
               092 W
                        A
DDFSTRT
               094 W
                        A
DDFSTOP
               096 W
                         A
                             P
DMACON
                                  Collision control
               098 W
CLXCON
                                  Interrupt Enable bits (clear or set bits)
               09A W
INTENA
               09C W
09E W
                                  Interrupt Request bits (clear or set bits)
INTREQ
                                  Audio, Disk, UART, Control
                              P
ADKCON
                                  Audio channel 0 location (High 5 bits)
AUDOLCH
               0A0
                     W
                                  Audio channel 0 location (Low 15 bits)
               0A2
AUD OLCL
                     W
                         A
               0A4
                                  Audio Channel O length
                     W
                                  Audio channel O Period
               0A6
                              P
                     W
AUD OPER
                                  Audio Channel O Volume
                              P
               0A8
                     W
AUD OVOL
                                  Audio channel O Data
               OAA W
                              P
AUDODAT
               0AC
                                  Audio channel 1 location (High 5 bits)
                         A
               0B0
                    W
AUD1LCH
                                   Audio channel 1 location (Low 15 bits)
               0B2
                     W
                         А
AUD1LCL
                                   Audio Channel 1 length
                              P
               0B4
                     W
AUD1LEN
                                   Audio channel 1 Period
                              P
               0B6
                     W
AUD1PER
                                   Audio Channel 1 Volume
               0B8
                     W
                              P
AUD1VOL
                                  Audio channel 1 Data
AUD1DAT
               0BA
                     W
               0BC
                                 Audio channel 2 location (High 5 bits)
                         A
                     W
AUD2LCH
```

```
Audio channel 2 location (Low 15 bits)
              0C2
     CL
                   W
                                  Audio Channel 2 length
              0C4 W
                             P
    LEN
                             Р
                                  Audio channel 2 Period
   ZPER
              0C6 W
                                  Audio Channel 2 Volume
                             P
  J2VOL
              0C8 W
                             P
                                  Audio channel 2 Data
              OCA W
 JD2DAT
              0CE
                                  Audio channel 3 location (High 5 bits)
Audio channel 3 location (Low 15 bits)
              ODO W
                        Α
AUD3LCH
           +
                   W
AUD3LCL
              0D2
                         A
                                  Audio Channel 3 length
AUD3LEN
               0D4
                             P
                                  Audio channel 3 Period
               0D6
                    W
                             P
AUD3PER
               0D8 W
                                  Audio Channel 3 Volume
                             P
AUD3VOL
                                  Audio channel 3 Data
              ODA W
                             Р
AUD3DAT
               ODE
                                  Bit plane 1 pointer (High 5 bits)
              OEO W
                       A
BPL1PTH
                                  Bit plane 1 pointer (Low 15 bits)
BPL1PTL
              0E2
                       A
         +
                    W
                                  Bit plane 2 pointer (High 5 bits)
BPL2PTH
         +
              0E4
                    TAT
                        A
                                  Bit plane 2 pointer (Low 15 bits)
BPL2PTL
              0E6
                    W
                         A
                                  Bit plane 3 pointer (High 5 bits)
BPL3PTH
         +
              0E8
                    W
                         A
                                  Bit plane 3 pointer (Low 15 bits)
              0EA
                    W
                         A
BPL3PTL
         +
                                  Bit plane 4 pointer (High 5 bits)
              0EC
BPL4PTH
         +
                    W
                         A
                                  Bit plane 4 pointer (Low 15 bits)
Bit plane 5 pointer (High 5 bits)
          +
               OEE
                         A
BPL4PTL
                    W
          +
               OF0
                    W
                         A
BPL5PTH
                                  Bit plane 5 pointer (Low 15 bits)
BPL5PTL
           +
               0F2
                    W
                         A
                                  Bit plane 6 pointer (High 5 bits)
           +
               0F4
                    W
                         A
BPL6PTH
                                  Bit plane 6 pointer (Low 15 bits)
               0F6
BPL6PTL
           +
                    W
                         A
                                  Bit plane 7 pointer (High 5 bits)
               0F8
                         A
BPL7PTH
           +
                    W
                                  Bit plane 7 pointer (Low 15 bits)
               OFA
BPL7PTL
                         A
           +
                    W
                                  Bit plane 8 pointer (High 5 bits)
BPL8PTH
          +
               OFC
                    W
                        A
                                  Bit plane 8 pointer (Low 15 bits)
BPL8PTL
              OFE
                    W
                        А
                                  Bit plane control register (misc control bits)
BPLCON0
               100
                    W
                         A D
                                  Bit plane control reg (scroll value PF1, PF2)
                         D
BPLCON1
               102
                    W
                                  Bit plane control reg (priority control)
Bit plane control reg (enhanced features)
Bit plane modulo (odd planes, or active-fetch
                         D
D
               104
BPLCON2
                    W
               106
                    W
BPLCON3
               108
                    W
                         A
BPL1MOD
                                  lines if bitplane scan-doubling enabled)
                                  Bit Plane modulo (even planes or inactive-fetch
BPL2MOD
               10A
                                  lines if bitplane scan-doubling enabled)
                                  Bit plane control reg (bitplane and sprite masks)
               10C
                           D
                     W
BPLCON4
          р
                                  Extended collision control register
          p
               10E
                           D
CLXCON2
                    W
                                  Bit plane 1 data (Parallel to serial convert)
                           D
               110
                    W
BPL1DAT
                                  Bit plane 2 data (Parallel to serial convert)
               112
                          D
BPL2DAT
                    TN
           3
                                  Bit plane 3 data (Parallel to serial convert)
BPL3DAT
           & 114
                    W
                          D
                                  Bit plane 4 data (Parallel to serial convert)
BPL4DAT
           & 116
                    TAT
                          D
                                  Bit plane 5 data (Parallel to serial convert)
Bit plane 6 data (Parallel to serial convert)
Bit plane 7 data (Parallel to serial convert)
Bit plane 8 data (Parallel to serial convert)
BPL5DAT
          & 118
                    W
                          D
                          D
BPL6DAT
          & 11A
                    W
                          D
          &p 11C
                    W
BPL7DAT
                          D
          &p 11E
                    W
BPL8DAT
                                  Sprite 0 pointer (High 5 bits)
SPR0PTH
          + 120
                    W
                         A
                                   Sprite 0 pointer (Low 15 bits)
SPR0PTL
           +
               122
                     W
                         A
                                  Sprite 1 pointer (High 5 bits)
           +
               124
                     W
                         A
SPR1PTH
               126
                                  Sprite 1 pointer (Low 15 bits)
SPR1PTL
           +
                     W
                         A
               128
                                  Sprite 2 pointer (High 5 bits)
                         A
SPR2PTH
           +
                     W
                                  Sprite 2 pointer (Low 15 bits)
              12A
                         Α
SPR2PTL
           +
                     W
                                  Sprite 3 pointer (High 5 bits)
              12C
                         A
SPR3PTH
           +
                     W
                                  Sprite 3 pointer (Low 15 bits)
SPR3PTL
              12E
                     W
                         A
                                  Sprite 4 pointer (High 5 bits)
SPR4PTH
           + 130
                    W
                         A
                                  Sprite 4 pointer (Low 15 bits)
SPR4PTL
           + 132
                     W
                         A
                                  Sprite 5 pointer (High 5 bits)
Sprite 5 pointer (Low 15 bits)
Sprite 6 pointer (High 5 bits)
Sprite 6 pointer (Low 15 bits)
                         A
SPR5PTH
           +
              134
                    W
              136
                    WA
           +
SPR5PTL
           +
              138
                    WA
SPR6PTH
              13A
                    W
                         A
SPR6PTL
           +
                                  Sprite 7 pointer (High 5 bits)
Sprite 7 pointer (Low 15 bits)
              13C
           +
                     W
                         A
SPR7PTH
                    W
                         A
SPR7PTL
           +
               13E
                                   Sprite 0 Vert-Horiz start position data
              140
                    W
                        A D
```

```
SPROCTL % 142 W
SPRODATA % 144 W
SPRODATB % 146 W
SPR1POS % 148 W
                                             Sprite 0 position and control data
Sprite 0 image data register A
                                A D
                               D
                                             Sprite 0 image data register B
Sprite 1 Vert-Horiz start position data
                                    D
                                 A D
             % 14A W
% 14C W
                                             Sprite 1 position and control data
Sprite 1 image data register A
                                 A D
SPR1CTL
                               D
D
SPR1DATA
             % 14E W
SPR1DATB
                                             Sprite 1 image data register B
                                             Sprite 2 Vert-Horiz start position data
              % 150 W
SPR2POS
                               A D
              % 152 W
                                             Sprite 2 position and control data
SPR2CTL
                               A D
                                D
D
                                            Sprite 2 image data register A
SPR2DATA % 154 W
SPR2DATB % 156 W
                                            Sprite 2 image data register B
                                            Sprite 3 Vert-Horiz start position data
SPR3POS
              % 158 W A D
              % 15A W
                                            Sprite 3 position and control data
SPR3CTL
                              A D
                                D
D
SPR3DATA % 15C W
                                            Sprite 3 image data register A
SPR3DATB % 15E W
                                            Sprite 3 image data register B
              % 160 W
                                            Sprite 4 Vert-Horiz start position data
SPR4POS
                              A D
              % 162 W
                                             Sprite 4 position and control data
                                A D
SPR4CTL
                                D
                                             Sprite 4 image data register A
Sprite 4 image data register B
Sprite 5 Vert-Horiz start position data
Sprite 5 position and control data
              % 164 W
SPR4DATA
SPR4DATB %
SPR5POS %
                   166
168
                           W
                                   D
                           W
                                 A D
                   16A W
SPR5CTL
               9
                                 A D
                                D
                                             Sprite 5 image data register A
                  16C
SPR5DATA
             8
                           W
SPR5DATB % 16E
                                             Sprite 5 image data register B
                           W
                                    D
             % 170 W
                                             Sprite 6 Vert-Horiz start position data
SPR6POS
                                 A D
SPR6CTL
              % 172 W
                                             Sprite 6 position and control data
                              A D
                               D
D
SPR6DATA % 174 W
                                             Sprite 6 image data register A
SPR6DATB % 176 W
                                             Sprite 6 image data register B
             % 178 W
                              A D
                                             Sprite 7 Vert-Horiz start position data
SPR7POS
                               A D
SPR7CTL
              % 17A W
                                             Sprite 7 position and control data
                  17A W D Sprite 7 positi
17C W D Sprite 7 image
180 W D Color table 00
182 W D Color table 02
186 W D Color table 03
188 W D Color table 04
18A W D Color table 05
18C W D Color table 07
190 W D Color table 07
190 W D Color table 09
194 W D Color table 10
196 W D Color table 10
198 W D Color table 11
198 W D Color table 12
19A W D Color table 13
19C W D Color table 14
19E W D Color table 15
1A0 W D Color table 16
1A2 W D Color table 17
1A4 W D Color table 18
1A6 W D Color table 20
1AA W D Color table 20
1AA W D Color table 21
1AC W D Color table 22
1AE W D Color table 23
1B0 W D Color table 24
1B2 W D Color table 24
1B2 W D Color table 25
1B4 W D Color table 27
1B8 W D Color table 27
1B8 W D Color table 28
1BA W D Color table 29
1BC W D Color table 30
1BE W D Color table 30
1BE W D Color table 31
1CO W A Highest number
1CO W A Highest number
                         W
                              D
                                             Sprite 7 image data register A
SPR7DATA % 17C
SPR7DATB % 17E W
                                  D
                                             Sprite 7 image data register B
COLOR00
COLOR01
COLOR02
COLOR03
COLOR04
COLOR05
COLOR06
COLOR07
COLOR08
COLOR09
COLOR10
COLOR11
COLOR12
COLOR13
COLOR14
COLOR15
COLOR16
COLOR17
COLOR18
COLOR19
COLOR20
COLOR21
COLOR22
COLOR23
COLOR24
COLOR25
COLOR26
COLOR27
COLOR28
COLOR29
COLOR30
COLOR31
             h 1C0 W A
h 1C2 W A
                                            Highest number count in horiz line (VARBEAMEN=1)
HTOTAL
HSSTOP
                                            Horiz line pos for HSYNC stop
                               A D
HBSTRT
              h 1C4 W
                                            Horiz line pos for HBLANK start
```

```
Horiz line pos for HBLANK stop
Highest numbered Vertical line (VARBEAMEN=1)
        h 1C6 W A D
HBSTOP
        h 1C8 W A
VTOTAL
                              Vert. line pos for VSYNC stop
VSSTOP
         h 1CA W A
                              Vert line for VBLANK start
                    A
VBSTRT
         h 1CC W
                              Vert line for VBLANK stop
          h 1CE W
                     A
VBSTOP
SPRHSTRT h 1D0 W
                              UHRES sprite vertical start
                      A
                               UHRES sprite vertical stop
SPRHSTOP
         h 1D2
                  W
                      A
                               UHRES bit plane vertical start
             1D4
                      A
BPLHSTRT
         h
                  W
            1D6
                               UHRES bit plane vertical stop
                      A
BPLHSTOP
         h
                  W
                               DUAL mode hires H beam counter write
             1D8
          h
                  W
                      A
HHPOSW
                               DUAL mode hires H beam counter read
HHPOSR
          h
             1DA
                  R
                      A
                               Beam counter control register (SHRES, UHRES, PAL)
                     A
BEAMCONO h
             1DC
                  W
             1DE W A
                              Horizontal Sync start (VARHSY)
HSSTRT
          h
             1EO W A
                               Vertical Sync start (VARVSY)
VSSTRT
          h
          h 1E2 W A
                              Horizontal position for Vsync on interlace
HCENTER
         h 1E4 W A D
                              Display window- upper bits for start, stop
DIWHIGH
         h 1E6 W A
                              UHRES bit plane modulo
BPLHMOD
                              UHRES sprite pointer (High 5 bits)
UHRES sprite pointer (Low 15 bits)
SPRHPTH
         +h 1E8 W A
SPRHPTL
         +h 1EA W A
                              VRam (UHRES) bit plane pointer (High 5 bits)
VRam (UHRES) bit plane pointer (Low 15 bits)
        +h 1EC W A
BPLHPTH
          +h 1EE W A
BPLHPTL
          1F0-1FA
P 1FC W A D
RESERVED
                              Fetch MODE register
FMODE
                               Can also indicate last 2 or 3 refresh cycles
NO-OP (NULL) 1FE
                                or the restart of the COPPER after lockup.
```

List of Registers ordered Alphabetically

```
P= new register in Pandora Chip Set
p= stuff added or changedin hires chips
H= new register in hires chips
h= stuff added or changed in hires chips
```

0 . 4 . 1 .

A=Agnus/Alice chip, D=Denise/Lisa chip, P=Paula chip

W=Write, R=Read, ER=Early read. This is a DMA data transfer to RAM, from either the Disk or from the Blitter . Ram timing requires data to be on the bus earlier than microprocessor read cycles. These transfers are therefore initiated by Agnus timing, rather than a read address on the register address bus (RGA).

```
NAME rev ADDR type chip Desription
```

| ADKCON ADKCONR | 09E 010 | |
|-------------------|------------|--|
| | | BIT# USE |
| | | 15 SET/CLR Set/Clear control bit. Determines if bits written with a 1 get set or cleared. Bits written with a zero are always unchanged. |
| | | 14-13 PRECOMP 1-0 CODE PRECOMP VALUE |
| | | 00 none 01 140 ns 10 280 ns 11 560 ns |
| | | 12 MFMPREC (1=MFM precomp 0=GCR precomp) 11 UARTBRK Forces a UART break (clears TXD) if true 10 WORDSYNC Enables disk read synchronizing on a word equal to DISK SYNC CODE, located in |
| | | address DSKSYNC (7E). 09 MSBSYNC Enables disk read synchronizing on the MSB |

(most signif bit). Appl type GCR 08 FAST Disk data clock rate control 1=fast(2us) 0=slow(4us) (fast for MFM or 2us GCR, slow for 4us GCR)

07 USE3PN Use audio channel 3 to modulate nothing
06 USE2P3 Use audio channel 2 to modulate period of channel 3
05 USE1P2 Use audio channel 1 to modulate period of channel 2
04 USE0P1 Use audio channel 0 to modulate period of channel 1

03 USE3VN Use audio channel 3 to modulate nothing

02 USE2V3 Use audio channel 2 to modulate volume of channel 3 01 USE1V2 Use audio channel 1 to modulate volume of channel 2

00 USEOV1 Use audio channel 0 to modulate volume of channel 1 NOTE If both period and volume are modulated on the same channel, the period and volume wil be alternated. First AUDxDAT word is used for V6-V0 of AUDxVOL Second AUDxDAT word is used for P15-P0 of AUDxPER this alternating sequence is repeated

Audio channel x location (High 5 bits) (old-3 bits) Audio channel x location (Low 15 bits) AUDxLCH h 0A0 W A 0A2 A AUDxLCL This pair of registers contains the 20 bit starting address (location) of Audio channel x (x=0,1,2,3) DMA data. This is not a pointer register and therefore only needs to be reloaded if a different memory location is to be outputted.

Audio Channel x length AUDXLEN OA4 W This register contains the length (number of words) of Audio Channel x DMA data.

Audio channel x Period AUDXPER h 0A6 This register contains the Period (rate) of Audio channel \times DMA data transfer. The minimum period is 124 color clocks. This means that the smallest number that should be placed in this register is 124. This corresponds to a maximum sample frequency of 28.86 khz. (124 decimal = 7C hex). For running with a horiz, frequency that is different (VARBEAMEN=1) the sampling frequency can be higher. Minimum period is (HTOTAL+21)/2 color clocks. See BEAMCONO for details of varbeamen.

P Audio Channel x Volume AUDXVOL 0A8 W This register contains the Volume setting for Audio Channel x. Bits 6,5,4,3,2,1,0 specify 65 linear volume levels as shown below.

> BITS 15-07 Not used Forces volume to max (64 ones, no zeros) 05-00 Sets one of 64 levels (000000=no output (111111=63 Ones, one zero)

Audio channel x Data P AUDXDAT OAA W This register is the Audio channel x (x=0,1,2,3) DMA data buffer. It contains 2 bytes of data (each byte is a twos complement signed integer) that are outputed sequentially (with digital to analog conversion) to the audio output pins. With maximum volume, each byte can drive the audio outputs with 0.8 volts(peak to peak, typ) The audio DMA channel controller automatically transfers data to this register from RAM. The Processor can also write directly to this register. When the DMA data is finished (words outputted=Length) and the data in this register has been used, an audio channel interrupt request

is set.

BEAMCONO H 1DC W A

Beam Counter control bits

Bit Function

| 15 14 13 1 12 11 10 9 | (unused) HARDDIS LPENDIS VARVBEN LOLDIS CSCBEN VARVSYEN VARHSYEN | 0-000000000000000000000000000000000000 | le compo |
|---|--|--|----------|
| 7 | VARBEAMEN DUAT | Š | |
| 5 | PAL | 0 | |
| 1 3 | VARCSYEN (unused, | formerly | BLANKEN) |
| 2 | CSYTRUE | O O | |
| 1 1 | VSYTRUE | 0 | |
| 0 | HSYTRUE | 0 | |

HARDDIS= This bit is used to disable the hardwire vertical and horizontal window limits. It is cleared upon reset. LPENDIS= When this bit is a low and LPE (BPLCONO, BIT 3) is enabled, the light-pen latched value (beam hit position) will be read by VHPOSR, VPOSR and HHPOSR. When the bit is a high the light-pen latched value is ignored and the actual beam counter position is read by VHPOSR, VPOSR and HHPOSR. VARVBEN= Use the comparator generated Vertical Blank (from VBSTRT, VBSTOP) to run the internal chip stuff-sending RGA signals to Denise, starting sprites, resetting light pen. It also disables the hard stop on the vertical display window.

LOLDIS= Disable long line/short line toggle. This is useful for DUAL mode where even multiples are wanted, or in any single display where this toggling is not desired. CSCBEN= The variable composite sync comes out on the HSY* pin, and the variable composite blank comes out on the VSY*

pin. The idea is to allow all the information to come out of the chip for a DUAL mode display. The normal monitor uses the normal composite sync, and the variable composite sync & blank come out the HSY* & VSY* pins. The bits VARVSYEN & VARHSYEN (below) have priority over this control bit.

VARVSYEN= comparator VSY -> VSY* pin. The variable VSY is set vertically on VSSTRT, reset vertically on VSSTOP, with the horizontal position for set & reset HSSTRT on short fields (all fields are short if LACE-O) and HCENTER on long

fields (all fields are short if LACE=0) and HCENTER on long fields (every other field if LACE=1)

VARHSYEN= comparator HSY -> HSY* pin. Set on HSSTRT value, reset on HSSTOP value.

VARBEAMEN= Enables the variable beam counter comparators to operate (allowing different beam counter total values) on the main horiz counter. It also disables hard display

stops on both horizontal & vertical.

DUAL= Run the horizontal comparators with the alternate horizontal beam counter, and starts the UHRES pointer chain with the reset of this counter rather than the normal one. This allows the UHRES pointers to come out more than once in a horizontal line, assuming there is some memory bandwidth left (It doesn't work in 640*400*4 interlace mode) Also, to keep the 2 displays synced, the horizontal line lengths should be multiples of each other. If you are amazingly clever, you might not need to do this. PAL= Set appropriate decodes (in normal mode) for PAL.

In variable beam counter mode this bit disables the long line/short line toggle- ends up short line.

VARCSYEN= enable CSY* from the variable decoders to come out the CSY* (VARCSY is set on HSSTRT match always, and also on HCENTER match when in vertical sync. It is reset on HSSTOP match when VSY*, and on both HBSTRT & HBSTOP matches during VSY. A reasonable composite can be generated by setting HCENTER half a horiz line from HSSTRT, and HBSTOP at (HSSTOP-HSSTRT) before HCENTER, with HBSTRT at (HSSTOP-HSSTRT) before HSSTRT.

HSYTRUE, VSYTRUE, CSYTRUE = These thange the polarity of the HSY*, VSY*, & CSY* pins to HSY', VSY, & CSY respectively for input & output.

- BLTxPTH h 050 W A Blitter Pointer to x (High 5 bits)

 BLTxPTL 052 W A Blitter Pointer to x (Low 15 bits)

 This pair of registers contains the 20 bit address of Blitter source (x=A,B,C) or dest. (x=D) DMA data.

 This pointer must be preloaded with the starting address of the data to be processed by the blitter. After the Blitter is finished it will contain the last data address (plus increment and modulo).
- BLTxMOD 064 W A Blitter Modulo x

 This register contains the Modulo for Blitter source(x=A,B,C) or Dest (x=D). A Modulo is a number that is automatically added to the address at the end of each line, in order that the address then points to the start of the next line.

 Each source or destination has it's own Modulo, allowing each to be a different size, while an identical area of each is used in the Blitter operation.
- BLTAFWM 044 W A Blitter first word mask for source A
 BLTALWM 046 W A Blitter last word mask for source A
 The patterns in these two registers are "anded" with the
 first and last words of each line of data from Source A into
 the Blitter. A zero in any bit overides data from Source A.
 These registers should be set to all "ones" for fill mode
 or for line drawing mode.
- BLTxDAT 074 W A Blitter source x data reg
 This register holds Source x (x=A,B,C) data for use
 by the Blitter. It is normally loaded by the Blitter
 DMA channel, however it may also be preloaded by
 the microprocessor.
- BLTDDAT 000 W A Blitter destination data register

 This register holds the data resulting from each word of
 Blitter operation until it is sent to a RAM destination.

 This is a dummy address and cannot be read by the micro.

 The transfer is automatic during Blitter operation.
- BLTCONO 040 W A Blitter control register 0
 BLTCONOL H 05A W A Blitter control register 0 (write lower 8 bits only)
 This is to speed up software-- the upper bits are often the same.
- BLTCON1 h 042 W A Blitter control register 1
 These two control registers are used together to control
 Blitter operations. There are 2 basic modes, area and line,
 which are selected by bit 0 of BLTCON1, as shown below.
 AREA MODE ("normal") LINE MODE (line draw)

BIT# BLTCONO BLTCON1 BIT# BLTCONO BLTCON1

```
15 ASH3
14 ASH2
                                                                       BSH3
                                   BSH3
                 15 ASH3
                                                                       BSH2
                       ASH2
                                   BSH2
                  14
                                                   13 ASH1
                                    BSH1
                  13
                       ASH1
                                                   12 ASHO
                                                                       BSH0
                  12
                      ASA0
                                    BSH0
                                                   11
                                                                       0
                                                        1
                  11
                      USEA
                                    0
                                                                        0
                                                   10
                                     0
                  10
                      USEB
                                                   09
                  09
                     USEC
                                    0
                                                   08
                                     0
                  08
                     USED
                                                  07 LF7
06 LF6
05 LF5
04 LF4
                                     DOFF
                                                                       DOFF
                  07
                      LF7
                                                                       SIGN
                  06
                      LF6
                                    0
                                                                       OVF
                       LF5
                                     0
                  05
                       LF4
                  04
                                    EFE
                                                   03 LF3
                                                                       SUL
                       LF3
                                     IFE
                  03
                                                   02
                                                        LF2
                                                                       AUL
                  02
                       LF2
                                    FCI
                                                   01 LF1
                                                                       SING
                                    DESC
                  01
                       LF1
                                    LINE (=0)
                                                   00 LF0
                                                                       LINE (=1)
                  00
                       LF0
                  ASH3-0 Shift value of A source
                  BSH3-0 Shift value of B source and line texture
                          Mode control bit to use Source A
                  USEA
                           Mode control bit to use Source B
                  USEB
                           Mode control bit to use Source C
                  USEC
                          Mode control bit to use Destination D
                  USED
                          Logic function minterm select lines
                  LF7-0
                          Exclusive fill enable Inclusive fill enable
                  EFE
                  TFE
                           Fill carry input
Descending (decreasing address) control bit
                  FCI
                  DESC
                           Line mode control bit
                  LINE
                           Line draw sign flag
                  SIGN
                           Line draw r/l word overflow flag
                  OVF
                           Line draw, Sometimes Up or Down (=AUD*)
                  SUD
                  SUL
                           Line draw, Sometimes Up or Left
                           Line draw, Always Up or Left
                  AUL
                           Line draw, Single bit per horiz. line
                  SING
                           Disables the D output- for external ALUs
                  DOFF
                           The cycle occurs normally, but the data bus is
                           tristate. (hires chips only)
                        Blitter start and size (window width, height)
          058 W A
                  This register contains the width and height of the blitter operation (in line mode width must =2, height = line length) Writing to this register will start the Blitter, and should
                  be done last, after all pointers and control registers have
                  been initialized.
                        15,14,13,12,11,10,09,08,07,06,05,04,03,02,01,00
                  BIT#
                         h9 h8 h7 h6 h5 h4 h3 h2 h1 h0, w5 w4 w3 w2 w1 w0
                  h=Height=Vertical lines (10 bits=1024 lines max)
                  w=Width =Horiz pixels (6 bits=64 words=1024 pixels max)
                  A Blitter H size & start (11 bit width)
Bit# 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
x x x x x x w10 w9 w8 w7 w6 w5 w4 w3 w2 w1 w0
BLTSIZH H O5E W A
                        Blitter V size (15 bit height)
15 14 12 12 11 10 09 08 07 06 05 04 03 02 01 00
                    A
                  Bit#
                         x h14 h13 h12 h11 h10 h9 h8 h7 h6 h5 h4 h3 h2 h1 h0
                  These are the blitter size registers for blits larger than
                  the earlier chips could accept. The original commands are
                  retained for compatibility. BLTSIZV should be written first,
                  followed by BLTSIZH, which starts the blitter. BLTSIZV need
                  not be rewritten for subsequent blits if the vertical size
                  is the same. max size of blit 32k pixels * 32k lines
                  x s should be written to 0 for upward compatibility.
```

BLTSIZE

BLTSIZV H 05C

BPLHDAT H 07A W ext logic UHRES bit plane pointer identifier

UHRES bit plane modulo BPLHMOD H 1E6 W A This is the number (sign extended) that is added to the UHRES bit plane pointer (BPLHPTL, H) every line, and then another 2 is added, just like the other modulos.

UHRES (VRAM) bit plane pntr (High 5 bits) BPLHPTH H 1EC W A A UHRES (VRAM) bit plane pntr (Low 15 bits) BPLHPTL H 1EE W When UHRES is enabled, this pointer comes out on the 2nd 'free' cycle after the start of each horiz. line. Its modulo is added every time it comes out. 'Free' means priority above the copper and below the fixed stuff (audio, sprites...) BPLHDAT comes out as an identifier on the RGA lines when the pointer address is valid so that external detectors can use this to do the special cycle for the VRAMs. The SHRHDAT gets the first and third free cycles.

UHRES bit plane vertical stop BPLHSTOP p 1D6 W A This controls the line when the data fetch stops for the BPLHPTH, L pointers.

> Bit# Name

15 BPLHWRM 14-11 unused

V10-V0 10-0

BPLHWRM= Swaps the polarity of ARW* when the BPLHDAT comes out so that external devices can detect the RGA and put things into memory (ECS and later versions).

UHRES bit plane vertical start BPLHSTRT H 1D4 W This controls the line when the data fetch starts for the BPLHPTH, L pointers. V10-V0 on DB10-0.

Bit plane x pointer (High 5 bits) 0E0 BPLxPTH x=1,2,3,45,6,7,80E4 0E8

0EC

OF0

0F4 P 0F8

P OFC

Bit plane x pointer (Low 15 bits) BPLxPTL 0E2

Address of Bit plane x (x=1,2,3,4,5,6,7,8) DMA data. This 0E6 pointer must be reinitalized by the processor or coprocessor 0EA to point to the beginning of Bit Plane data every vertical OEE blank time.

OF2

0F6

P OFA

P OFE

110 W D Bit plane x data (Parallel to serial convert) BPLxDAT

These registers receive the DMA data fetched from RAM 112 114

by the Bit Plane address pointers described above. They may also be written by either micro. 116

They act as a 8 word parallel to serial buffer 118

for up to 8 memory "Bit Planes". (x=1-8 The parallel to serial conversion is triggered whenever bit plane #1 11A P 11C

is written, indicing the completion of all bit planes P 11E for that word (16/32/64 pixels). The MSB is output first, and is therefore always on the left.

Bit plane modulo (odd planes) Bit Plane modulo (even planes) A A 108 W BPL1MOD 10A W BPL2MOD These registers contain the Modulos for the odd and even bit planes. A Modulo is a number that is automatically added to the address at the end of each line, in order that the address then points to the start of the next line. Since they have separate modulos, the odd and even bit planes may have sizes that are different from each other, as well as different from the Display Window size. If bitplane scan-doubling is enabled, BPL1MOD serves as the primary bitplane modulus and BPL2MOD serves as the alternate. Lines whose LSBs of beam counter and DIWSTRT match are designated primary, whereas lines whose LSBs don't match are

| BPLCON0 BPLCON1 | | | | A D D | Bit | plane | control | reg. (misc control bits) reg. (horiz. scroll control) |
|--------------------|---|-----|---|-------|-----|-------|---------|---|
| BPLCON2 | O | 104 | W | D | Bit | plane | control | reg. (new control bits) |
| BPLCON3 | | | | | Bit | Plane | control | reg. (enhanced features) |
| BPLCON4 | - | | | D | Bit | Plane | control | reg.(display masks) |

designated alternate.

These registers control the operation of the Bit Planes and various aspects of the display.

| BIT# | √BPLCON0 | √BPLCON1 | BPLCON2 /BPLCON3 | ∕BPLCON4 |
|---|--|------------------|---|--|
| BIT# 15 14 13 12 11 10 09 08 07 06 05 04 03 | ✓BPLCON0 HIRES BPU2 BPU1 BPU0 HAM DPF COLOR GAUD UHRES SHRES BYPASS=0 BPU3=0 LPEN | ✓BPLCON1 | x BANK2=0 ZDBPSEL2 BANK1=0 ZDBPSEL1 BANK0=0 ZDBPSEL0 PF20F2=0 ZDBPEN PF20F1=1 ZDCTEN PF20F0=1 KILLEHB CCT=0 RDRAM=0 x SOGEN=0 SPRES1=0 PF2PRI SPRES0=0 PF2P2 BRDRBLNK=0 | BPLAM7=0 BPLAM6=0 BPLAM5=0 BPLAM4=0 BPLAM3=0 BPLAM2=0 BPLAM1=0 BPLAM0=0 ESPRM7=0 ESPRM6=0 ESPRM5=0 |
| 02 | LACE CERSY | PF1H4 2 PF1H3 | PF1P2 | OSPRM6=0 OSPRM5=0 |
| 00 | ×ECSENA=0 | PF1H2 along | PF1P0 EXTBLKEN=(| OSPRM4=0 |

x= don't care; but drive to 0 for upward compatibility ! =0/=1 bit values initialized by RST_ pin going low.

HIRES=High resolution(640*200/640*400interlace) mode
BPUx =Bit plane use code 0000-1000 (NONE thru 8 inclusive)
HAM=Hold and Modify mode, now using either 6 or 8 bitplanes.

New HAM mode is invoked when this bit is set and BPU =1000. Now available in all resolutions.

DPF=Double playfield (PF1=odd PF2=even bit planes)

now available in all resolutions

(If BPU=6 and HAM=0 and DPF=0 a special mode is defined that allows bitplane 6 to cause an intensity reduction of the other 5 bitplanes. The color register output selected by 5 bitplanes is shifted to half intensity by the 6th bitplane. This is called EXTRA-HALFBRITE Mode.

COLOR= enables color burst output signal.

GAUD=Genlock audio enable. This level appears on the ZD pin on Denise during all blanking periods, unless ZDCLK bit is set.

UHRES= ultrahi res enables the UHRES pointers (for 1k*1k) (also needs bits in DMACON) (hires chips only)

```
Disables hard stops for vert., horiz. display windows SHRES= super-hi-res mode (35nS pixel width)
    BYPASS= bitplanes are scrolled and prioritized normally, but
            bypass color table and 8 bit wide data appear on
            R(7:0).
    LPEN =Light pen enable (reset on power up)
    LACE =Interlace enable (reset on power up)
    ERSY =External Resync (HSYNC, VSYNC pads become inputs)
            (reset on power up)
    ECSENA = When low(default), the following bits in BPLCON3 are
            disabled: BRDRBLNK, BRDNTRAN, ZDCLKEN, BRDSPRT, and
            EXTBLKEN. These 5 bits can always be set by writing
            to BPLCON3, however there effects are inhibited until
            ECSENA goes high. This allows rapid context switching
            between pre-ECS viewports and new ones.
    PF2Hx= Playfield 2 horizontal scroll code, x=0-7
PF1Hx= Playfield 1 horizontal scroll code, x=0-7
where PFyH0=LSB=35nS=1 SHRES pixel (bits have been
           renamed, old PFyHO now PFyH2, etc.). Note that the
           scroll range has been quadrupled to allow for wider
           (32 or 64 bit) bitplanes.
    ZDBPSELx= 3 bit field which selects which Bit plane is to be
           used for ZD when ZDBBPEN is set;000 selects BP1 and 111
           selects BP8.
    ZDBPEN= causes ZD pin to mirror bitplane selected by
            ZDBPSELx bits. This does not disable the ZD mode
            defined by ZDCTEN, but rather is sed" with it.
                   ZD pin to mirror bit #15 or the active entry
    ZDCTEN=
                   high color table. When ZDCTEN is reset ZD
    reverts to mirroring color(0). KILLEHB= disables Extra Half Brite mode.
    RDRAM= causes color table addresses to read the color table
           instead of writing to it.
    SOGEN= when set causes SOG output pin to go high
    PF2PRI= gives Playfield 2 priority over Playfield 1.
    PF2Px= Playfield 2 priority code (with resp. to sprites)
    PF1Px= Playfield 1 priority code (with resp. to sprites)
    BANKx= selects one of eight color table banks, x=0-2.
    PF2OFx= determine bitplane color table offset when playfield 2
            has priority in dual playfield mode:
   PF2OF
                  AFFECTED BITPLANE
                                             | OFFSET
| 2 | 1 | 0 | | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | | (decimal)
1 | 0 | 1 | | - | - | 1 | - | - | - | - | 32
           1 0
   LOCT= dictates that subsequent color palette values will be
         written to a second 12-bit color palette, constituting
          the RGB low-order bits. Writes to the normal high-order
         color palette are automatically copied to the low-order
          for backwards compatibility.
   SPRESx= determine resolution of all 8 sprites (x=0,1):
   SPRES1 | SPRESO | SPRITE RESOLUTION
          0 | ECS defaults (LORES, HIRES=140nS, SHRES=70nS
                  | LORES (140nS)
                  | HIRES (70nS)
```

1 | 1 | SHRES (35nS)

BRDRBLNK= "border area" is blanked instead of color(0).

****RESET BY ECSENA*****

BRDNTRAN= "border area" is non-transparent (ZD pin is low when border is displayed).

****RESET BY ECSENA****

ZDCLKEN= ZD pin outputs a 14MHZ clock whose falling edge coincides with high-res(7MHZ) video data. This bit when set disables all other ZD functions.

RESET BY ECSENA*

BRDRSPRT= enables sprites outside the display window.

****RESET BY ECSENA****

EXTBLKEN= causes BLANK output to be programmable instead of reflecting internal fixed decodes.

****RESET BY ECSENA****

BPLAMx= this 8 bit field is XOR'ed with the 8 bitplane color address, thereby altering the color address sent to the color table(x=1-8).

ESPRMx= 4 bit field provides the 4 high order color table address bits for even sprites: SPR0, SPR2, SPR4, SPR6. Default value is 0001 binary. (x=7-4)

OSPRMx= 4 bit field provides the 4 high order color table address bits for odd sprites: SPR1, SPR3, SPR5, SPR7. Default value is 0001 binary. (x=7-4)

CLXCON 098 W D Collision control

This register controls which Bitplanes are included (enabled) in collision detection, and their required state if included. It also controls the individual inclusion of odd numbered sprites in the collision detection, by logically ORing them with their corresponding even numbered sprite. Writing to this register resets the bits in CLXCON2.

CLXCON2 P 10C W D Extended Collision Control
This register controls when bitplanes 7 & 8 are included in collision detection, and their required state if included.
Contents of this register are reset by a write to CLXCON.
***** BITS INITIALIZED BY RESET *****

| BIT# | FUNCTION | DESCRIPTION |
|-------------------|----------------|--|
| | | |
| 15-08 07 06 | ENBP8 ENBP7 | unused Enable Bit Plane 8 (Match reqd. for collision) Enable Bit Plane 7 (Match reqd. for collision) |
| 05-02 01 | - MVBP8 | unused Match value for Bit Plane 8 collision |

MVBP7 Match value for Bit Plane 7 collision

Note: Disabled Bit Planes cannot prevent collisions.

Therefore if all bitplanes are disabled, collisions will be continuous, regardless of the match values.

CLXDAT 00E R D Collision data reg.(Read and clear)

This address reads (and clears) the collision detection register. The bit assignments are below.

NOTE: Playfield 1 is all odd numbered enabled bit planes.

Playfield 2 is all even numbered enabled bit planes

BIT# COLLISIONS REGISTERED

15 not used

14 Sprite 4 (or 5) to Sprite 6 (or 7)

13 Sprite 2 (or 3) to Sprite 6 (or 7)

12 Sprite 2 (or 3) to Sprite 4 (or 5)
11 Sprite 0 (or 1) to Sprite 6 (or 7)
10 Sprite 0 (or 1) to Sprite 4 (or 5)
09 Sprite 0 (or 1) to Sprite 2 (or 3)
08 Playfield 2 to Sprite 6 (or 7)

O8 Playfield 2 to Sprite 6 (or 7)
O7 Playfield 2 to Sprite 4 (or 5)
O6 Playfield 2 to Sprite 2 (or 3)
O5 Playfield 2 to Sprite 0 (or 1)
O4 Playfield 1 to Sprite 6 (or 7)

O3 Playfield 1 to Sprite 4 (or 5)
O2 Playfield 1 to Sprite 2 (or 3)
O1 Playfield 1 to Sprite 0 (or 1)
O0 Playfield 1 to Playfield 2

COLORxx 180-1BE W COLOR table xx

There are thirty-two (32) of these registers (xx=00-31) and together with the banking bits they address the 256 locations in the color palette. There are actually two sets of color registers, selection of which is controlled by the LOCT register bit. When LOCT=0 the 4 MSB of RED, GREEN, and BLUE video data are selected along with the T bit for genlocks. The low order set of registers is also selected simultaneously, so that the 4 bit values are automatically extended to 8 bits. This provides compatibility with old software. If the full range of palette values are desired, then LOCT can be set high and independant values for the 4 LSB of RED, GREEN, and BLUE can be written. The low order color registers do not contain a transparency(T) bit. The Table below shows the color register bit usage.

07,06,05,04, 03,02,01,00 15,14,13,12, 11,10,09,08, BIT # G7 G6 G5 G4 B7 B6 B5 B4 R7 R6 R5 R4 T X X X LOCT=0 B3 B2 B1 B0 R3 R2 R1 R0 G3 G2 G1 G0 X X LOCT=1

T = TRANSPARENCY R = RED G = GREEN B = BLUE X = UNUSED

T bit of COLOROO thru COLOR31 sets ZD_ pin HI when that color is selected in all video modes.

COPCON h 02E W A Coprocessor control register

This is a 1 bit register that when set true, allows the Coprocessor to access the Blitter hardware. This bit is cleared by power on reset, so that the Coprocessor cannot access the Blitter hardware.

BIT# NAME FUNCTION

O1 CDANG Coprocessor danger mode. Allows coprocessor access to all RGA registers if true.

(if 0, access to RGA>7E)

(on old chips- access to only RGA>3E if CDANG=1) (see VPOSR)

| COLOITT | A Coprocessor restart at second location these addresses are strobe addresses, that when written to cause the Coprocessor to jump indirect using the address contained in the First or Second Location registers described below. The Coprocessor itself can write to these |
|---------|---|
| | addresses, causing it's own jump indirect. |

| COPILCH h | 080 | W | A Coprocessor | first location reg (High 5 bits) (old-3 bits) |
|-----------|-----|-----|---------------|---|
| CODITCI | 002 | TAT | A Conrocessor | first location req. (LOW 15 DITS) |
| COP2LCH h | 084 | W | A Coprocessor | second location reg. (High 5 bits) (old-3 bits) |
| COP2LCL | 086 | TAT | A Coprocessor | second location reg(LOW 15 DIUS) |
| | | Th | ese registers | contain the jump addresses described above. |

A Coprocessor inst. fetch identify
This is a dummy address that is generated by the Coprocessor COPINS 08C W whenever it is loading instructions into it's own instruction register. This actually occurs every Coprocessor cycle except for the second (IR2) cycle of the MOVE instruction. The Three types of instructions are shown below. Move immediate to dest MOVE

Wait until beam counter is equal to, or greater than. WAIT (keeps Coprocessor off of bus until beam position has been reached)

Skip if beam counter is equal to, or greater than. SKIP (skips following MOVE inst. unless beam position has been reached)

| | MOV | Ε | WAIT U | JNTIL | SKIP | IF |
|---|---|------|--|---|--|---|
| BIT# 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 | MOVI IR1 X X X X X X DA8 DA7 DA6 DA5 DA4 DA3 DA2 DA1 | E | WAIT U IR1 VP7 VP6 VP5 VP4 VP3 VP2 VP1 VP0 HP8 HP7 HP6 HP5 HP4 HP3 HP2 | IR2 BFD * VE6 VE5 VE4 VE3 VE2 VE1 VE0 HE8 HE7 HE6 HE5 HE4 HE3 HE2 | SKIP IR1 VP7 VP6 VP5 VP4 VP3 VP2 VP1 VP0 HP8 HP7 HP6 HP5 HP4 HP3 HP2 | IR2 BFD * VE6 VE5 VE4 VE3 VE2 VE1 VE0 HE8 HE7 HE6 HE5 HE4 HE3 HE2 |
| 00 | 0 | RD00 | 1 | 0 | 1 | 1 |

IR1=First instruction register

IR2=Second instruction register DA =Destination Address for MOVE instruction. Fetched during

IR1 time, used during IR2 time on RGA bus.
RD =RAM Data moved by MOVE instruction at IR2 time

directly from RAM to the address given by the DA field.

VP =Vertical Beam Position comparison bit

HP =Horizontal Beam Position comparison bit

VE =Enable comparison(mask bit) HE =Enable comparison (mask bit)

* NOTE BFD=Blitter finished disable. When this bit is true, the Blitter Finished flag will have no effect on the Coprocessor. When this bit is zero the Blitter Finished flag must be true

(in addition to the rest of the bit comparisons) before the Coprocessor can exit from its wait state, or skip over an instruction. Note that the V7 comparison cannot be masked.

The Coprocessor is basically a 2 cycle machine that requests the bus only during odd memory cycles. (4 memory cycles per in) It has priority over only the Blitter and Micro.

There are only three types of instructions, MOVE immediate, WAIT until ,and SKIP if. All instructions require 2 bus cycles (and two instruction words). Since only the odd bus cycles are requested, 4 memory cycle times are required per instruction. (memory cycles are 280 ns)

There are two indirect jump registers COP1LC and COP2LC. These are 20 bit pointer registers whose contents are used to modify the program counter for initalization or jumps. They are transfered to the program counter whenever strobe addreses COPJMP1 or COPJMP2 are written. In addition COP1LC is automatically used at the beginning of each vertical blank time.

It is important that one of the jump registers be initalized and it's jump strobe address hit, after power up but before Coprocessor DMA is initalized. This insures a determined startup address, and state.

DDFSTRT 092 W DDFSTOP 094 W

A Display data fetch start (Horiz.Position)
A Display data fetch stop (Horiz.Position)
These registers control the horizontal timing of the beginning and end of the Bit Plane DMA display data fetch.
The vertical Bit Plane DMA timing is identical to the Display windows described above.

The Bit Plane Modulos are dependent on the Bit Plane horizontal size, and on this data fetch window size.

Register bit assignment

BIT# 15,14,13,12,11,10,09,08,07,06,05,04,03,02,01,00
USE X X X X X X X X H8 H7 H6 H5 H4 H3 X

(X bits should always be driven with 0 to maintain upward compatability)

The tables below show the start and stop timing for different register contents.

DDFSTRT(Left edge of display data fetch)

| PURPOSE | | | | н8, | 17, | н6, | Н5, | H4 | 1 | 5 |
|---------|-----|-------|---|-----|-----|-----|------|----|---|---|
| | | | - | | | | | | | |
| Extra w | ide | (max) | * | 0 | 0 | 1 | 0 | 1 | Ŏ | |
| W | ide | | | 0 | 0 | 1 | 1 | 0 | | |
| nor | mal | | | 0 | 0 | 1 | 2400 | - | | |
| nar | row | | | 0 | 1 | 0 | 0 | 0 | | |

DDFSTOP (Right edge of display data fetch)

| PURPOSE | Н8, | H7, | н6, | Н5, | H4 |
|------------|-----|-----|-----|-----|----|
| | | | | | |
| narrow | 1 | 1 | 0 | 0 | 1 |
| normal | 1 | 1 | 0 | 1 | 0 |
| wide (max) | 1 | 1 | 0 | 1 | 1 |

Note that these numbers will vary with variable beam counter mode set. (The maxes & mins, that is)

DIWSTRT 08E W A D Display Window Start (upper left vert-hor pos)

DIWSTOP 090 W A D Display Window Stop (lower right vert-hor pos)

These registers control the Display window size and position, by locating the upper left and lower right corners.

BIT# 15,14,13,12,11,10,09,08,07,06,05,04,03,02,01,00

USE V7 V6 V5 V4 V3 V2 V1 V0 H9 H8 H7 H6 H5 H4 H3 H2

Were

DIWSTRT is vertically restricted to the upper 2/3

of the display (V8=0), and horizontally restricted to the left 3/4 of the display(H8=0).*

DIWSTOP is vertically restricted to the lower 1/2

of the display (V8=/=V7), and horizontally restricted to the right 1/4 of the display(H8=1).*

* Poof.. (See DIWHIGH for exceptions)

DIWHIGH p 1E4 W A D Display Window upper bits for start, stop

This is an added register for the Hires chips, and allows
larger start & stop ranges. If it is not written, the above
(DIWSTRT, STOP) description holds. If this register is written
last in a sequence of setting the display window, it sets
direct start & stop positions anywhere on the screen.
It doesn't affect the UHRES pointers.

Bit# 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

x x H10 H1 H0 V10 V9 V8 x x H10 H1 H0 V10 V9 V8

were (stop) / 1/8 (start)

Don't care (x) bits should always be written to 0 to maintain upwards compatibility. H1 and H0 values define 70nS and 35nS increments respectively, and are new LISA bits.

NOTE: In all 3 display window registers, horizontal bit positions have been renamed to reflect HIRES pixel increments, e.g. what used be called HO is now referred to as H2.

DMACON 096 W A D P DMA control write(clear or set)

DMACONR 002 R A P DMA control (and blitter status) read

This register controls all of the DMA channels, and contains

Blitter DMA status bits.

| BIT# | FUNCTION | DESCRIPTION |
|----------------------|------------------|--|
| 15 | SET/CLR | Set/Clear control bit. Determines if bits written with a 1 get set or cleared. Bits written with a zero are unchanged. |
| 14 13 12 11 | | Blitter busy status bit (read only) Blitter logic zero status bit.(read only) |
| | BLTPRI | Blitter DMA priority(over CPU micro) (also called "Blitter Nasty") (disables /BLS pin, preventing micro from stealing any bus cycles while blitter DMA is running) |
| 09 | DMAEN | Enable all DMA below (also UHRES dma) Bit Plane DMA enable |
| 08 07 | BPLEN COPEN | Coprocessor DMA enable |
| 06 | BLTEN | Blitter DMA enable Sprite DMA enable |
| 05 04 | SPREN DSKEN | Disk DMA enable |
| 03 | AUD3EN | Audio channel 3 DMA enable |
| 02 | AUD2EN AUD1EN | Audio channel 2 DMA enable Audio channel 1 DMA enable |
| 00 | AUD0EN | Audio channel O DMA enable |
| | | |

| DSKPTH DSKPTL | h 020 022 | W A Disk pointer (High 5 bits) (old-3 bits) W A Disk pointer (Low 15 bits) This pair of registers contains the 20 bit address of Disk DMA data. These address registers must be initalized by the processor or coprocessor before disk DMA is enabled. |
|-------------------|-------------------------------|--|
| DSKLEN | 024 | This register contains the length (number of words) of Disk DMA data. It also contains 2 control bits. These are a DMA enable bit, and a DMA direction(read/write) bit. BIT# |
| | | 15 DMAEN Disk DMA Enable 14 WRITE Disk Write(RAM to Disk) if 1 13-0 LENGTH Length (# of words) of DMA data. |
| DSKDAT DSKDATR | 026 008 | W P Disk DMA Data write ER P Disk DMA Data read (early read dummy address) This register is the Disk-DMA data buffer. It contains 2 bytes of data that are either sent to (write) or received from (read) the disk. The write mode is enabled by bit 14 of the LENGTH register. The DMA controller automatically transfers data to or from this register and RAM, and when the DMA data is finished (Length=0) it causes a Disk Block Interrupt. See interrupts below. |
| DSKBYTR | 01A | This register is the Disk-Microprocessor data buffer. Data from the disk (in read mode) is loaded into this register one byte at a time, and bit 15 (DSKBYT) is set true. BIT# 15 DSKBYT Disk byte ready (reset on read) 14 DMAON DMAEN(DSKLEN) & DMAEN(DMACON) & DSKEN(DMACON) 13 DISKWRITE Mirror of bit 14 (WRITE) in DSKLEN 12 WORDEQUAL This bit true only while DSKSYNC register equals the data from disk 11-08 0 Not used 07-00 DATA Disk byte data |
| DSKSYNC | 07E | W P Disk sync register, holds the match code for disk read synchronization. See ADKCON bit 10 |
| FMODE (| P 1FC | W Memory Fetch Mode This register controls the fetch mechanism for different types of Chip Ram accesses: |
| | Bit# | Function Description |
| | 15 14 | SSCAN2 global enable for sprite scan-doubling. BSCAN2 enables use of 2nd P/F modulus on an alternate line basis to support bitplane scan-doubling. |
| | 13-04 03 02 01 00 | - unused SPAGEM Sprite Page Mode (double CAS) SPR32 Sprite 32 Bit Wide Mode BPAGEM Bitplane Page Mode (double CAS) BPL32 Bitplane 32 Bit Wide Mode |
| | BPAGE | M BPL32 Bitplane Fetch Increment Memory Cycle Bus Width |
| | 0 0 1 1 | 0 by 2 bytes (as before) normal CAS 16 1 by 4 bytes normal CAS 32 0 by 4 bytes double CAS 16 1 by 8 bytes double CAS 32 |

| | SPAGEM | SPR32 | Sprite Fetch Inc | crement Mem | ory Cycle | Bus Width |
|-------------------|------------------|---|--|---|--|---|
| | 0 0 1 1 | 0 1 0 1 | by 2 bytes (as) by 4 bytes by 4 bytes by 8 bytes | nor dou | | 16 32 16 32 |
| | HBSTOP HBSTRT | 1C6 1C4 | W D Horizon | tal STOP pos tal STaRT po | sition osition | |
| | | | Bits 7-0 containespectively, for 280nS increment control in 35nS | or programme s. Bits 10-8 | ed horizontal 3 provide a f: | branking in |
| | | BIT# | FUNCTION | DESCRIPTION | V | |
| | | 15-11 10 09 08 07 06 05 04 03 02 01 | H2 0 H1 H0 H10 H9 0 H8 1 H7 0 H6 1 H5 0 H4 0 H3 1 | (unused) 140nS 70nS 35nS 35840nS 17920nS 8960nS 4480nS 2240nS 1120nS 560nS 280nS | 08 SF 2F | |
| HCENTER | H 1E2 | This i | Horizontal page 15 necessary for the series See BEAMCONG | interlace mo | ode with vari | able beam |
| HHPOSR HHPOSW | H 1DA H 1D8 | R A W A This is | DUAL mode hi DUAL mode hi DUAL mode hi s the secondary aster mode, trigg risons for HBSTRI HTOTAL for bits) | res H beam beam beam counter | counter write r for HRES pointers | & doing the |
| HSSTOP | н 1С2 | W A Sets | Horiz line p | YOT SAILC S | COD (IIIIOIIII I | for bits) |
| HSSTRT | H 1DE | W A | Horiz line p f of color clocks EAMCONO for detail | osition for some s | tart (HTOTAL | for bits) |
| HTOTAL | н 1СО | W A Bit# 3 (x's s Horiz PAL bs | Highest cold 15 14 13 12 11 10 x x x x x x x should be driven | or clock cou 0 09 08 07 0 0 x x h8 h 1 to 0 for up 1 any + 1 280 1 to thigh, lo 1 be this man | nt in horiz 16 05 04 03 02 07 h6 h5 h4 h3 ward compatibles increments ong line/short | nne 1000 h2hl pility) s. If the t line toggle will |
| INTREQ INTREQR | | This These by th | P Interrupt Representation P Interrupt represents and personal Properties Pro | equest bits s interrupt led by the p the next re Both a set | (read) request bits processor, and egister, they and clear ope | (or flags). d if enabled may cause eration |
| INTENA | 09A | W | P Interrupt E | nable bits (| (clear or set | bits) |

INTENAR 01C R

P Interrupt Enable bits Read This register contains interrupt enable bits. The bit assignment for both the request, and enable registers is given below.

BIT# FUNCT LEVEL DESCRIPTION

| 15 | SET/CLR | | Set/Clear control bit. Determines if bits written with a 1 get set or cleared. Bits written with a zero are always unchanged. |
|-----|---------|---|---|
| 14 | INTEN | | Master interrupt (enable only , no request) |
| 13 | EXTER | 6 | External interrupt |
| 12 | DSKSYN | 5 | Disk Sync register (DSKSYNC) matches Disk data |
| 11 | RBF | 5 | Serial port Receive Buffer Full |
| 10 | AUD3 | 4 | Audio channel 3 block finished |
| 09 | AUD2 | 4 | Audio channel 2 block finished |
| 0.8 | AUD1 | 4 | Audio channel 1 block finished |
| 07 | AUD0 | 4 | Audio channel O block finished |
| 06 | BLIT | 3 | Blitter finished |
| 05 | VERTB | 3 | Start of Vertical blank |
| 04 | COPER | 3 | Coprocessor |
| 03 | PORTS | 2 | I/O Ports and timers |
| 02 | SOFT | 1 | Reserved for software initiated interrupt. |
| 01 | DSKBLK | 1 | Disk Block finished |
| 00 | TBE | 1 | Serial port Transmit Buffer Empty |

JOYODAT OOA R JOY1DAT OOC R

D Joystick-mouse 0 data (left vert,horiz)
D Joystick-mouse 1 data (right vert,horiz)
These addresses each read a 16 bit register. These in turn are loaded from the MDAT serial stream and are clocked in on the rising edge of SCLK. MLD* output is used to parallel load the external parallel-to-serial converter. This in turn is loaded with the 4 quadrature inputs from each of two game controller ports (8 total) plus 8 miscellaneous control bits which are new for LISA and can be read in upper 8 bits of LISAID.
Register bits are as follows:

Mouse counter usage(pins 1,3 =Yclock, pins 2,4 =Xclock)
BIT# 15,14,13,12,11,10,09,08 07,06,05,04,03,02,01,00
JOYODAT Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0 X7 X6 X5 X4 X3 X2 X1 X0
JOY1DAT Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0 X7 X6 X5 X4 X3 X2 X1 X0

O=left controller pair, 1=right controller pair. (4 counters total). The bit usage for both left and right addresses is shown below. Each 6 bit counter(Y7-Y2, X7-X2) is clocked by 2 of the signals input from the mouse serial stream. Starting with first bit received:

| Serial bit | Name | Description |
|------------|------|---------------------------------------|
| | | |
| 0 | MOH | JOYODAT Horizontal Clock |
| 1 | MOHQ | JOYODAT Horizontal Clock (quadrature) |
| 2 | MOV | JOYODAT Vertical Clock |
| 3 | MOVQ | JOYODAT Vertical Clock (quadrature) |
| 4 | M1H | JOY1DAT Horizontal Clock |
| 5 | M1HQ | JOY1DAT Horizontal Clock (quadrature) |
| 6 | MlV | JOY1DAT Vertical Clock |
| 7 | M1VO | JOY1DAT Vertical Clock (quadrature) |

Bits 1 and 0 of each counter (Y1-Y0,X1-X0) may be read to determine the state of the related input signalpair. This allows these pins to double as joystick switch inputs. Joystick switch closures can be deciphered as follows:

| Directions | Pin# | counter bits | |
|------------|------|------------------------------|----|
| | | | |
| Forward | 1 | Y1 xor Y0 (BIT#09 xor BIT#08 | 3) |

Left X1 xor X0 (BIT#01 xor BIT#00) 2 Back X1 Right Write to all 4 Joystick-mouse counters at once. D 036 W JOYTEST Mouse counter write test data: BIT# 15,14,13,12,11,10,09,08 07,06,05,04,03,02,01,00 JOYODAT Y7 Y6 Y5 Y4 Y3 Y2 xx xx X7 X6 X5 X4 X3 X2 xx xx JOY1DAT Y7 Y6 Y5 Y4 Y3 Y2 xx xx X7 X6 X5 X4 X3 X2 xx xx Denise/Lisa (video out chip) revision level D LISAID H 07C The original Denise (8362) does not have this register, so whatever value is left over on the bus from the last cycle will be there. ECS DENISE(8373) returns hex(FC) in the lower 8 bits. LISA returns hex (F8). The upper 8 bits of this DFFO7C register are loaded from the serial mouse bus, and are reserved for future hardware implentation. The 8 low-order bits bits are encoded as follows: BIT# Description Lisa/Denise/ECS Denise Revision level(decrement to 7-4 bump revision level, hex F represents 0th rev. level). maintain as a 1 for future generation 3 When low indicates AA feature set(LISA)
When low indicates ECS feature set(LISA or ECS Denise) maintain as a 1 for future generation P Pot counter data left pair (vert, horiz) POTODAT h 012 P Pot counter data right pair (vert, horiz) POTIDAT h 014 These addresses each read a pair of 8 bit pot counters. (4 counters total). The bit assignment for both addresses is shown below. The counters are stopped by signals from 2 controller connectors(left-right) with 2 pins each. BIT# 15,14,13,12,11,10,09,08 07,06,05,04,03,02,01,00 RIGHT Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0 X7 X6 X5 X4 X3 X2 X1 X0 LEFT Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0 X7 X6 X5 X4 X3 X2 X1 X0 CONNECTORS PAULA loc. dir. sym pin RIGHT Y RY 9 33 5 RIGHT X RX 32 9 36 LEFT Y LY 35 5 LEFT X LX With normal (NTSC or PAL) horiz. line rate, the pots will give a full scale (FF) reading with about 500kohms in one frame time. With proportionally faster horiz line times, the counters will count proportionally faster. This should be noted when doing variable beam displays. 034 W P Pot Port (4 bit) Direction and Data, POTGO and Pot Counter start. Pot pin data read P POTINP 016 R This register controls a 4 bit bi-directional I/O port that shares the same 4 pins as the 4 pot counters above. DESCRIPTION BIT# FUNCT I/O data Paula pin 33
Output enable for Output enable for Paula pin 33 OUTRY 15 DATRY 14 Output enable for Paula pin 32 13 OUTRX I/O data Paula pin 32 12 DATRX

```
Output enable for Paula pin 36
                           OUTLY
                                      I/O data Paula pin 36
                    10
                           DATLY
                                      Output enable for Paula pin 35
                    09
                           OUTLX
                                      I/O data Paula pin 35
                           DATLX
                    08
                                      not used
                    07 - 01
                            X
                                      Start pots (dump capacitors, start counters)
                           START
                                Refresh pointer
            028 W A
REFPTR
                    This register is used as a Dynamic RAM refresh address generator. It is writeable for test purposes only, and
                    should never be written by the microprocesor.
                                Serial Port Data and stop bits write
SERDAT
                    This address writes data to a Transmit data buffer.
                    Data from this buffer is moved into a serial shift register
                    for output transmission, whenever it is empty. This sets the
                    Interrupt Request TBE (transmit buffer empty). A stop bit
                    must be provided as part of the data word. The length of the data word is set by the position of the stop bit. BIT# 15,14,13,12,11,10,09,08,07,06,05,04,03,02,01,00 USE 0 0 0 0 0 S D8 D7 D6 D5 D4 D3 D2 D1 D0 note: S= stop bit =1 , D= data bits
                                Serial Port Data and Status read
           018 R
SERDATR
                     This address reads data from a Receive data buffer.
                     Data in this buffer is loaded from a receiving shift register
                     whenever it is full. Several interrupt request bits are also
                     read at this address, along with the data, as shown below.
                     BIT#
                                            Serial port receiver overun
                     15
                                            Serial port Receive Buffer Full (mirror)
                     14
                            RBF
                                           Serial port Transmit Buffer Empty (mirror)
Serial port Transmit shift reg. empty
                            TBE
                     13
                            TSRE
                     12
                                           RXD pin receives UART serial data for direct
                     11
                            RXD
                                           bit test by the micro
Not used
                     10
                             X
                                            Stop bit
                     09
                            STP
                                           Stop bit if LONG, Data bit if not.
                     08
                         STP-DB8
                                           Data bit
                           DB7
                                           Data bit
                     06
                            DB6
                                           Data bit
                     05
                            DB5
                                           Data bit
                     04
                            DB4
                                           Data bit
                     03
                            DB3
                                           Data bit
                     02
                            DB2
                                            Data bit
                     01
                            DB1
                                            Data bit
                            DB0
                           P Serial Port Period and control
            032 W
                     This register contains the control bit LONG reffered to above, and a 15 bit number defining the serial port Baud Rate. If this number is N, then the Baud Rate is
                     1 bit every (N+1)*.2794 Microseconds.
                     BIT#
                                           Defines Serial Receive as 9 bit word.
                     15
                              LONG
                                           Defines Baud Rate=1/((N+1)*.2794 microsec)
                     14-00 RATE
                  W ext logic UHRES sprite identifier & data
 SPRHDAT H 078
                     This identifies the cycle when this pointer address is on the
                     bus accessing the memory.
                                 UHRES sprite pointer (High 5 bits)
                     A
                  W
 SPRHPTH H 1E8
                     A
                                 UHRES sprite pointer (Low 15 bits)
 SPRHPTL H 1EA
                  W
                     This pointer is activated in the 1st & 3rd 'free' cycles
                      (see BPLHPTH, L) after horiz line start. It increments
                     for the next line.
```

SPRHSTOP H 1D2 W A UHRES sprite vertical display stop

Bit# 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 SPRHWRM x x x x v10 v9 v8 v7 v6 v5 v4 v3 v2 v1 v0

SPRHWRM= Swaps the polarity of ARW* when the SPRHDAT comes out so that external devices can detect the RGA and put things into memory. (ECS and later chips only)

SPRHSTRT H 1D0 W A UHRES sprite vertical display start

Bit# 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

x x x x x v10 v9 v8 v7 v6 v5 v4 v3 v2 v1 v0

SPRXPTH 120 W A Sprite x pointer (High 5 bits)

SPRXPTL 122 W A Sprite x pointer (Low 15 bits)

This pair of registers contains the 20 bit address of Sprite x (x=0,1,2,3,4,5,6,7) DMA data. These address registers must be initialized by the processor or coprocessor every vertical blank time.

SPRxPOS 140 W A D Sprite x Vert-Horiz start position data

BIT# SYM FUNCTION

15-08 SV7-SV0 Start vertical value. High bit (SV8) is in SPRxCTL reg below.

07-00 SH10-SH3 Sprite horizontal start value. Low-order 3 bits are in SPRxCTL register below. If SSCAN2 bit in FMODE is set, then disable SH10 horizontal coincidence detect. This bit is then free to be used by ALICE as an individual scan double enable.

SPRxCTL p 142 W A D Sprite x position and control data

| BIT# 15-08 07 06 05 04 03 02 01 00 | SYM EV7-EV0 ATT SV9 EV9 SH1=0 SH0=0 SV8 EV8 SH2 | End (stop) vert. value. low 8 bits Sprite attach control bit (odd sprites only) start vert. value 10th bit end (stop) vert. value 10th bit start horiz. value, 70nS increment start horiz. value, 35nS increment Start vert. value 9th bit End (stop) vert. value 9th bit start horiz. value, 140nS increment |
|---|--|--|
| | | the state of the s |

These 2 registers work together as position, size and feature Sprite control registers. They are usually loaded by the Sprite DMA channel, during horizontal blank, however they may be loaded by either processor any time. Writing to SPRxCTL disables the corresponding sprite.

SPRxDATA 144 W D Sprite x image data register A SPRxDATB 146 W D Sprite x image data register B

These registers buffer the Sprite image data. They are usually loaded by the Sprite DMA channel but may be loaded by either processor at any time. When a horizontal coincidence occurs the buffers are dumped into shift registers and serially outputed to the display, MSB first on the left. Note: Writing to the A buffer enables (arms) the sprite. Writing to the SPRxCTL register disables the sprite. If enabled, data in the A and B buffers will be output whenever the beam counter equals the sprite horizontal position value in the SPRxPOS register. In lowres mode,

The DATB bits are the 2SBs (worth 2) for the color re: and MSB for SHRES. DATA bits are LSBs of the pixels. STREQU 038 Strobe for horiz sync with VB (vert. blank) and Ex STRVBL 03A Strobe for horiz sync with VB STRHOR 03C DP Strobe for horiz sync STRLONG h 03E D Strobe for identification of long horz. line (228 CC) One of the first 3 strobe addresses above, it is placed on the RGA bus during the first refresh time slot. The 4th strobe shown above is used during the second refresh time slot of every other line, to identify lines with long counts (228- NTSC, HTOTAL+2- VARBEAMEN=1 hires chips only). There are 4 refresh time slots and any not used for strobes will leave a null (1FE) address on the RGA bus. A VBSTOP H 1CE W Vertical line for VBLANK stop A VBSTRT H 1CC W Vertical line for VBLANK strt (V10-0 <- D10-0) Affects CSY* pin if BLANKEN=1 & VSY* Pin if CSCBEN=1 (see BEAMCONO) VPOSR p 004 R Read Vert most sig. bits (and frame flop) A A Write Vert most sig. bits (and frame flop)
BIT# 15,14,13,12,11,10,09,08, 07,06,05,04,03,02,01,00
USE LOF I6 I5 I4 I3 I2 I1 I0,LOL -- -- -- -- v10 v9 V8 А VPOSW 02A LOF=Long frame (auto toggle control bit in BPLCONO) IO-I6 chip identification: 8361 (regular) or <math>8370 (fat) (agnus-ntsc) = 108367 (pal) or 8371 (fat-pal) (agnus-pal) = 008372(fat-hr) (agnushr), thru rev. 4 = 20 PAL, 30 NTSC 8372(fat-hr) (agnushr), rev. 5 = 21 PAL, 31 NTSC 8374 (alice) = 22 PAL, 32 NTSC / 23/33LOL=Long line bit. When low, it indicates short raster line. 62 v9,v10-- hires chips only (20,30 identifiers) VHPOSR 006 R Read Vert and Horiz Position of beam, or lightpen A Write Vert and Horiz Position of beam, or lightpen 15,14,13,12,11,10,09,08,07,06,05,04,03,02,01,00 V7 V6 V5 V4 V3 V2 V1 V0,H8 H7 H6 H5 H4 H3 H2 H1 VHPOSW 02C BIT# RESOLUTION=1/160 OF SCREEN WIDTH (280 NS) VSSTOP H 1CA Vert. position for VSYNC stop. See BEAMCONO for more details. (V10-0 <- D10-0) VSSTRT H 1E0 W Vert. position for VSYNC start VTOTAL H 1C8 Highest numbered vertical line (VARBEAMEN=1) It's the line number to reset the counter, so there's this many + 2 in a field. The exception is if the LACE bit is set (BPLCONO), in which case every other field is this many +2 & the short field is this

many + 1.

1 sprite pixel is 1 bitplane pixel wide. In HRES a SHRES mode, 1 sprite pixel is 2 bitplane pixels.